AN1152

DGD2136M Application Information

The DGD2136M is a highly integrated three phase gate driver IC used to drive N-Channel MOSFETs or IGBTs. Below (Figure 1) is an example application of using the DGD2136M with IGBTs to provide three half-bridge circuits used to drive a three-phase motor; typical motor applications are AC Induction motors, PMSMs, and BLDC motors. In this discussion, the important parameters needed to design in the DGD2136M are discussed. The main sections are bootstrap resistors, diodes, capacitor selection, gate driver component selection, and decoupling capacitor value.

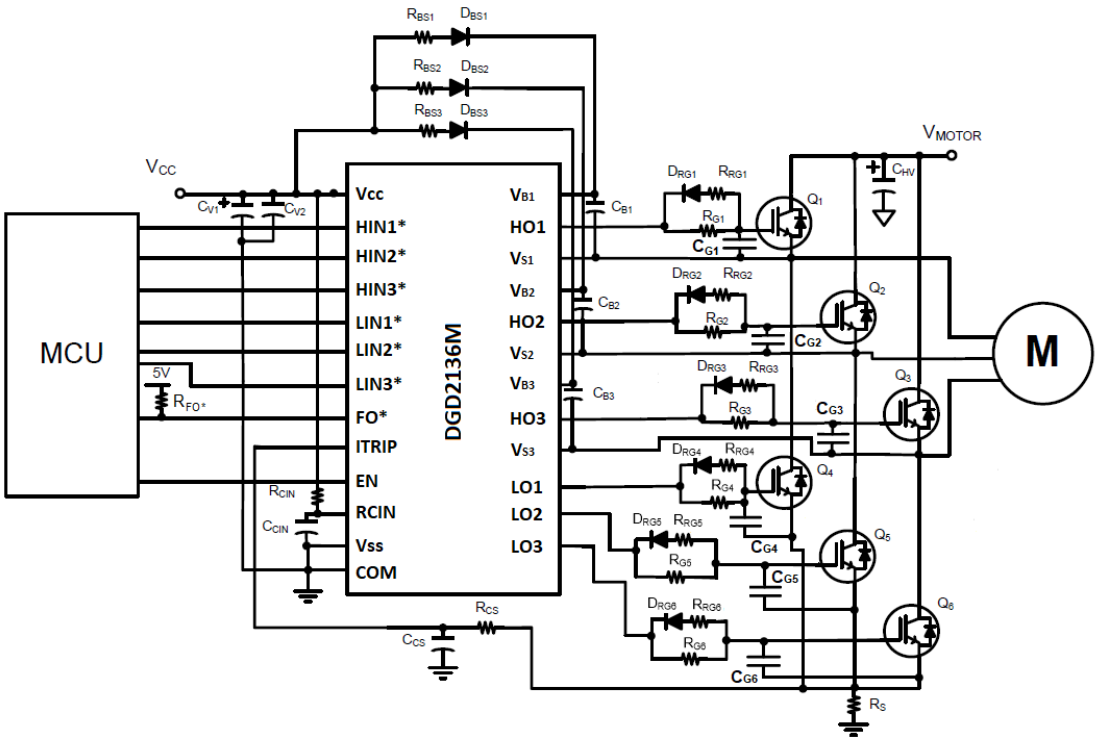

Figure 1. DGD2136M application example

Bootstrap Component Selection

Bootstrap Resistor

Considering Figure 1, when the low side IGBT (Q4, Q5, or Q6) turns on, Vs pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}, or C_{B3}) is charged. When the high-side IGBT (Q1, Q2, or Q3) is turned on, V_S swings above Vcc and the charge on the bootstrap capacitor (C_B) provides current to drive the IC high-side gate driver. The first charge of C_B from Vcc through the bootstrap resistor (R_{BS1}, R_{BS2}, or R_{BS3}) and bootstrap diode (D_{BS1}, D_{BS2}, or D_{BS3}) occurs when power is first applied and the low side turns on the first time. At this time the charge current is the largest as typically C_B is not discharged fully at each cycle.

A bootstrap resistor (R_{BS}) is included in the bootstrap circuit to limit the inrush current that charges C_B when Vs pulls below Vcc. This inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on Vs and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{BS} and C_{BS} as well as Vcc level. The aim in resistor selection for the application is to slow down the inrush current but have minimal effect on the RC time constant of charging C_{BS}.

Typically, values for R_{BS} are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the V_{BS} turn on. Figures 2-5 illustrate the effect of different R_{BS} values.

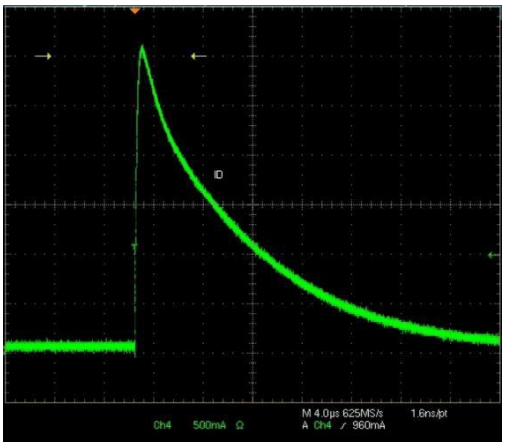

Figure 2. Bootstrap Peak inrush current ≈3A with RBS=3Ω, CBS=2.2µF

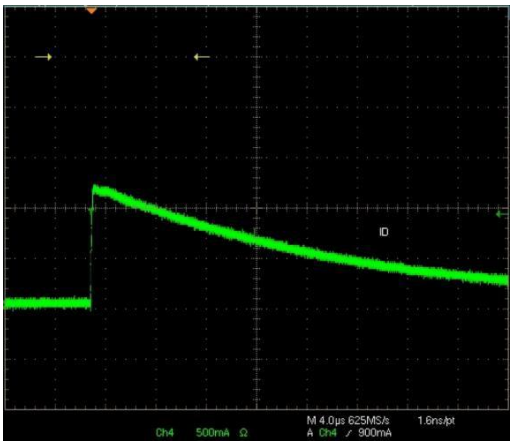

Figure 3. Bootstrap Peak inrush current ≈1.2A with RBS=10Ω, CBS=2.2µF

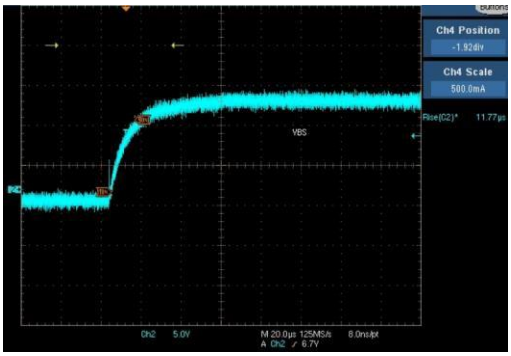

Figure 4. VBS Rise Time (11.8µs) with RBS=3Ω, CBS=2.2µF

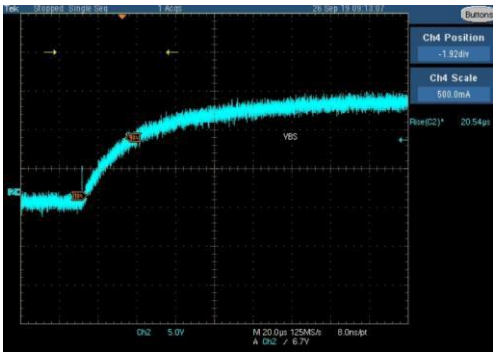

Figure 5. VBS Rise Time (20.5µs) with RBS=10Ω, CBS=2.2µF

Bootstrap Diode

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the V_S node. The diode's current rating is simply the product of total charge (QT) required by the HVIC (High Voltage Integrated Circuit) and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the C_{BS} cap. A 1A ultrafast recovery diode is typical for DGD2136M applications.

Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage (V_{GS_min}) must be greater than the UVLO of the high-side circuit, specifically V_{BSUV-} level. Therefore, if V_{GS_min} is the minimum gate-source voltage such that:

$V_{GS\_min} > V_{BSUV-}$

Then:

$\Delta V_{BS} = Vcc - V_f - V_{GS\_min} - V_X$

Where:
- Vcc is the supply voltage to the DGD2136M
- V_f is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET or IGBT

V_X is calculated as the current seen across low-side MOSFET multiplied by its R_{DS_ON} and is simply V_{CE_ON} at the specific output current if an IGBT were used instead.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (QT) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{H\_ON}$

Where:

Q_G = gate charge of power device
Q_{LS} = level shift charge required per cycle
T_{H_ON} = high-side on time
I_{LK_N} = sum of all leakages that include:
- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{Q_BS}: Quiescent current for high side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; depending on the process technology, it could range anywhere from 3-20nC for 500V to 1200V process respectively. Assuming a value of 10nC for the 600V process should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$C_{B\_min} \geq Q_T / \Delta V_{BS}$

Example using IGBT, IRGB4066

HVIC=DGD2136M

Vcc = 15V
Iout = 40A
T_{H_ON} = 50µs
V_{CE_max} = ~2.0V
Q_G = 225nC
I_{GSS}/I_{GES} = 200nA
I_{LK_DB} = 100µA
I_{LK_IC} = 10µA
I_{Q_BS} = 130µA

From equations 1, 2 and 3:

ΔV_{BS} = 15V- 1.0V-10V-(2V) = 2V

$Q_T = Q_G + Q_{LS} + (I_{LK\_N} * T_{H\_ON})$

= 225nC + 10nC + 12nC

= 247nC

Thus C_{BS} min = 247nC/2V = 124nF.

The bootstrap capacitor calculated in the above example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used. In addition, if the added margin is significantly small still, such that it is lower than 0.47µF, the minimal value should be brought up to this value. Utilizing values lower than this could result in overcharging of the bootstrap capacitor especially during –VS transients.

Typically for motor driver applications C_{BS} = 1µF to 10µF are used; also, it is recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Gate Resistor Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and to perform this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI; too slow a rise/fall time will increase switching losses in the MOSFET.

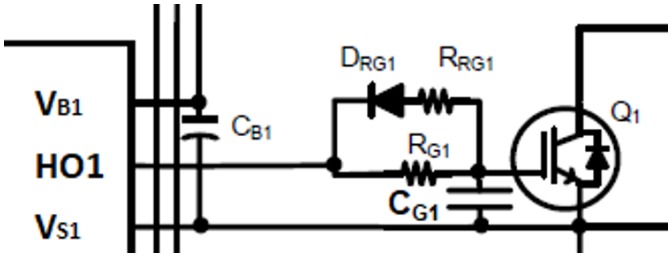

Figure 6. Phase1 Gate Drive Components for DGD2136M

Considering the phase 1 gate driver components for DGD2136M in Figure 6, with the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{G1} and charge the IGBT gate capacitor, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through R_{RG1} and D_{RG1} to the driver in the IC to VS. So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application. Generally, for motors the switching speed is slower, and the application has more inherent noise, higher values are recommended, for example R_G = 20Ω - 100Ω.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example, for the circuit in Figure 1, R_{RG1}=R_{RG4}, D_{RG1}=D_{RG4}, and R_{G1}=R_{G4}.

The gate to source capacitors (C_{G1} in Figure 6) are used to minimize unexpected shoot-through in the half-bridge. This shoot-through can decrease efficiency or even damage IGBTs or MOSFETs; this phenomenon is discussed further on page 7.

Fault timing Circuit

The DGD2136M contains an overcurrent protection (OCP) circuit that shuts off all the outputs when ITRIP goes above 500mV (this will be current sense resistor value X maximum current), see Figure 7. When ITRIP is above 500mV, the OCP circuit pulls the FO* pin to GND.

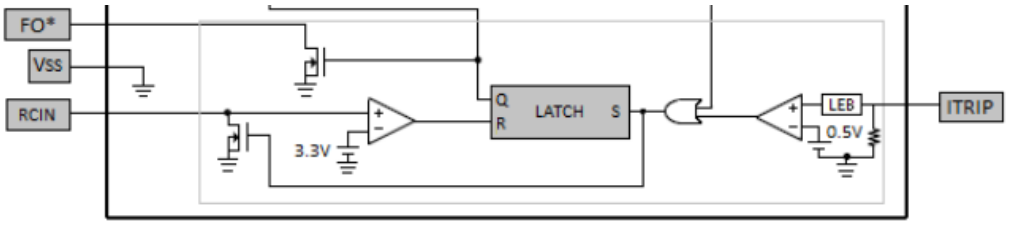

Figure 7. DGD2136M OCP Circuit

External to the IC (see Figure 8), the FO* line is pulled up to 5V (often from the control board) by R_{FO*}; 5kΩ is a typical value for this pullup resistor. After FO* is pulled low and there is no longer a fault (ITRIP is below 500mV), there is a fault clear time determined by the RC constant of R_{CIN} and C_{CIN} values (see Figure 8). This is a system design decision, but an example and typical value is given in the datasheet:

Fault Clear Time	t_{FLTCLR}	—	1.6	—	ms	C_{RCIN} = 1nF, R_{RCIN} = 2MΩ

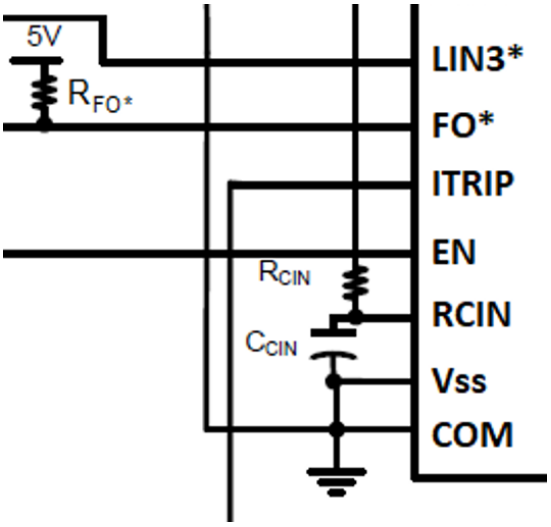

Figure 8. DGD2126M Fault timing circuit

Current Sense Filter

Even during normal operation in a half-bridge there is significant noise on the current sense line. Hence an RC current sense filter is suggested to filter out some of the higher frequency noise.

The cut-off frequency of the low pass filter is given by:

$fc = 1/2\pi(R_{CS})(C_{CS})$

For example: if R_{CS}=1kΩ and C_{CS}=1nF, the Fc = 159kHz, filtering out to about 6µs pulse.

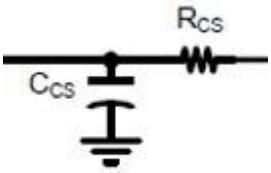

Figure 9. Current sense filter

Decoupling Capacitor Selection

For optimal operation, Vcc decoupling is crucial for all gate driver ICs including the DGD2136M. With poor decoupling, Vcc can drop when switching and for greater Vcc drop the IC can go into UVLO. In the configuration shown in Figure 1, with V_{SS} and COM connected close to the IC (at GND), two decoupling capacitors are recommended C_{V1} and C_{V2} (see Figure 10), both connected from Vcc-GND. C_{V1} can be a larger electrolytic, for example 47µF, 50V and does not need to be right next to the IC. But C_{V2} should be a low ESR ceramic capacitor placed close to the Vcc pin. This component provides stability when Vcc is quickly pulled down with load; typical values are 0.1µF to 1µF. If V_{SS} and COM are not shorted at the IC and may be different potential, it is suggested to have one ceramic capacitor from Vcc-COM and another capacitor from Vcc-V_{SS}.

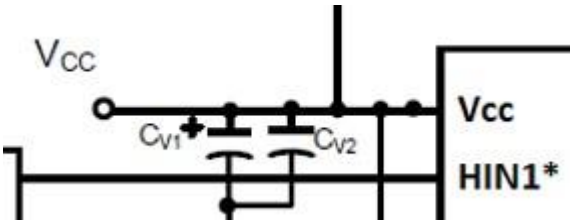

Figure 10. Decoupling capacitors on the DGD2136M

Input Resistors

The IC PWM inputs, HIN1*-HIN3* and LIN1*-LIN3*, are high impedance inputs with a pull up resistors for both inputs to 5V from internal regulator, (see Figure 11). The pull up resistors have a value of approx. 50kΩ.

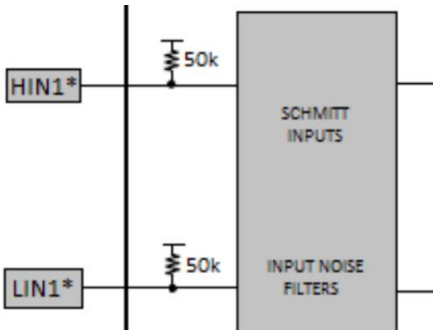

Figure 11. Input resistors for the DGD2136M

Matching Gate Driver with MOSFET or IGBT

IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, their ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2136M the drive current is I_{O+}=200mA typical and I_{O-}=350mA typical.

For a given MOSFET/IGBT with the known drive current of the DGD2136M, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example with Diodes' DGTD65T15H2TF, 650V IGBT, Qg = 61nC; and with the DGD2136M I_{O+}/I_{O-}, tr = 305ns and tf = 174ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

Unexpected shoot-through with dV_{DS}/d_t

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/d_t (see Figure 12) is often the cause of unexplained shoot through in the half-bridge circuit. Depending on the ratio of the C_{GS}/ C_{GD} , when the dV_{DS}/d_t across low-side MOSFET (Q2) occurs (i.e when high-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the VS line and the power ground.

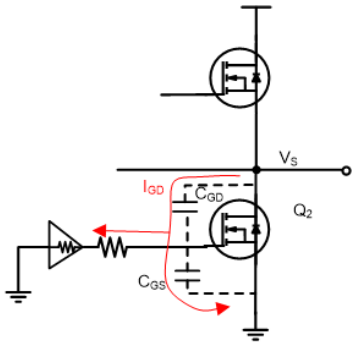

Figure 12. Unexpected shoot through with dV_{DS}/d_t

Considering Figure 12,

$I_{GD} = C_{GD}$ x dV_{DS}/d_t

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. Also an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/C_{GD}.

Minimum Pulse Requirement

For superior noise performance, the DGD2136M has an input filtering time of 250ns. Also, the DGD2136M has a typical propagation delay of 330ns. With the prop delay of the DGD2136M, delay time from gate resistors, and rise/fall from the MOSFETs/IGBTs, for optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU. As a rule of thumb, this minimum pulse should be 2 x deadtime or 660ns.

During typical operation, the DGD2136M will respond to an input pulse greater than 250ns (approximate value from the RC input filter response). Hence for an input pulse greater than 250ns approximately the IC will follow the pulse as expected; and for an input pulse less than 250ns, there will be no response from the IC.

PCB layout suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation which can arise from poor layout. Figure 13 shows a single phase half-bridge schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 13, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and decoupling capacitor (C_D) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

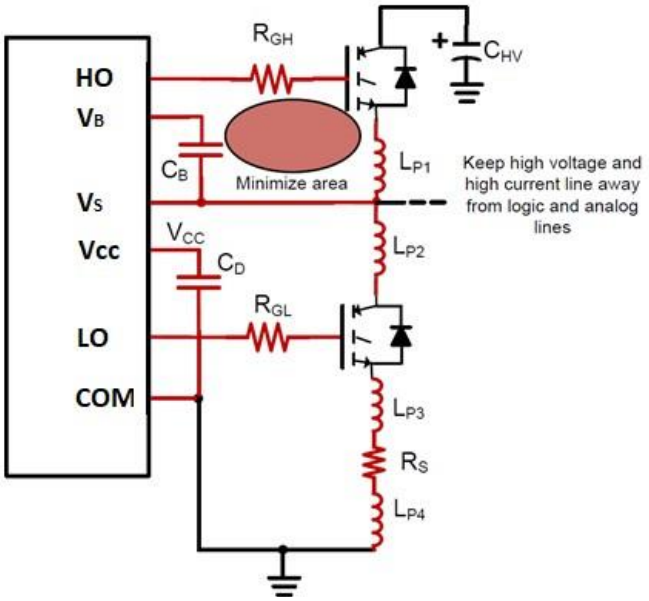

Figure 13. Layout suggestions for single phase of three phase system

DGD2136M in three phase half-bridge PCB layout example (below)

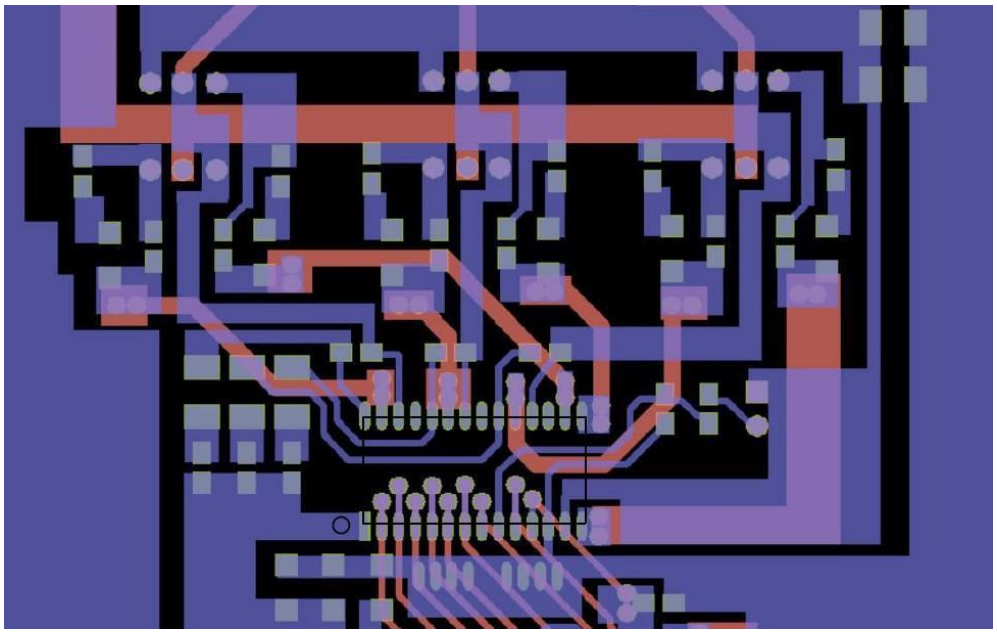

Fig 14. Layout of the schematic shown in Figure 1, DGD2136M in SOIC28, IGBTs in TO220 Packages

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