AN1194

DGD2003/DGD1003 Application Note

David Toro, Bipolar Business Unit, Diodes Incorporated

The DGD2003 and DGD1003 Half-Bridge Gate Drivers optimally drive MOSFET and IGBT gates. Below (Figure 1) is an example application using the DGD2003 with MOSFETs to make three Half-Bridge circuits used to drive a three-phase motor. Typical motor applications are AC induction motors, PMSMs, and BLDC motors. Both devices can also be used in power supplies. DGD2003 and DGD1003 differ in maximum operating voltage and package options. This application note discusses the important parameters needed to design in the DGD2003 and DGD1003. The main sections are bootstrap resistor, diode, and capacitor selection; Gate Driver component selection; decoupling capacitor discussion; and PCB layout suggestions.

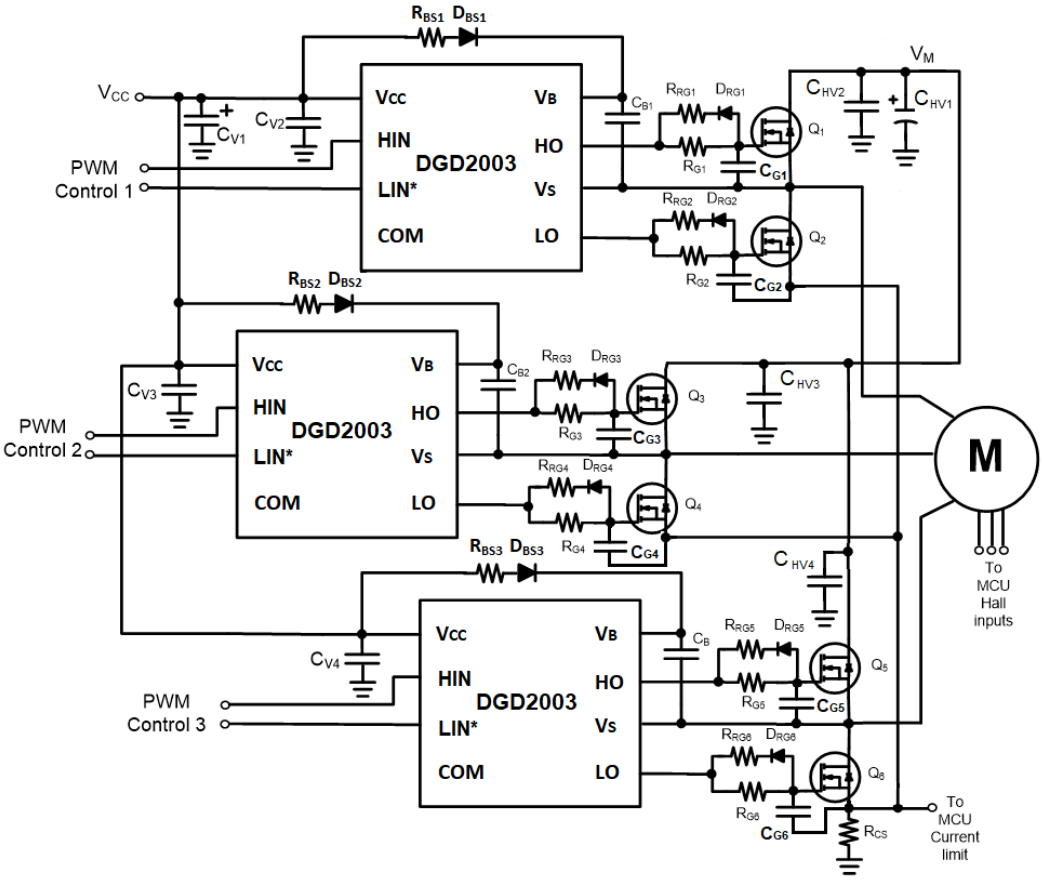

Figure 1. Three-Phase Motor Driver Application Example of DGD2003

Bootstrap Component Selection

Bootstrap Resistor

Considering Figure 1 when the Low-Side MOSFET (Q_2, Q_4, or Q_6) turns on, V_S pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}, or C_{B3}) is charged. When the High-Side MOSFET (Q_1, Q_3, or Q_5) turns on, V_S swings above Vcc and the charge on the bootstrap capacitor (C_B) provides current to drive the IC High-Side Gate Driver. The first charge of the C_B from Vcc through the bootstrap resistor (R_{BS1}, R_{BS2}, or R_{BS3}) and bootstrap diode (D_{BS1}, D_{BS2}, or D_{BS3}) occurs when power is first applied and the low-side turns on for the first time. At this time, the charge current is the largest as typically C_B is not discharged fully at each cycle.

A bootstrap resistor (R_{BS}) is included in the bootstrap circuit to limit the inrush current that charges C_B when V_S pulls below Vcc; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spikes on V_S and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of R_{BS} and C_{BS}, as well as Vcc level. The aim for the resistor selection in the application is to slow down the inrush current yet have minimal effect on the R_C time constant of the charging C_{BS}.

Typically, values for R_{BS} are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the V_{BS} turning on. Figures 2-5 illustrate the effect of different R_{BS} values.

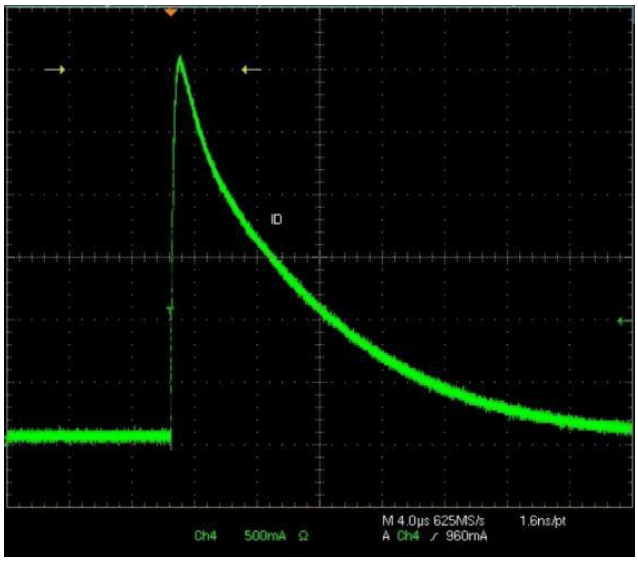

Figure 2. Bootstrap Peak inrush current ≈ 3A with R_{BS}=3Ω, C_{BS}=2.2µF

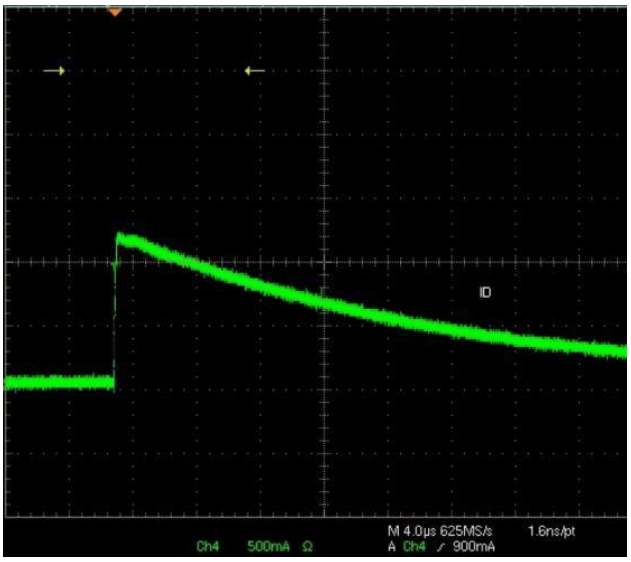

Figure 3. Bootstrap Peak inrush current ≈ 1.2A with R_{BS}=10Ω, C_{BS}=2.2µF

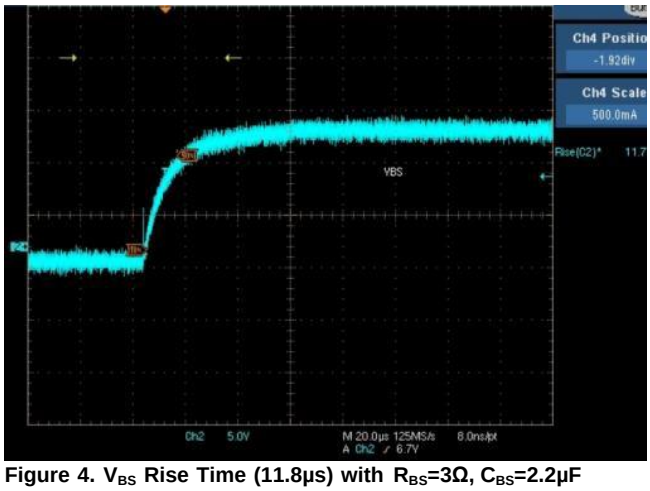

Figure 4. V_{BS} Rise Time (11.8µs) with R_{BS}=3Ω, C_{BS}=2.2µF

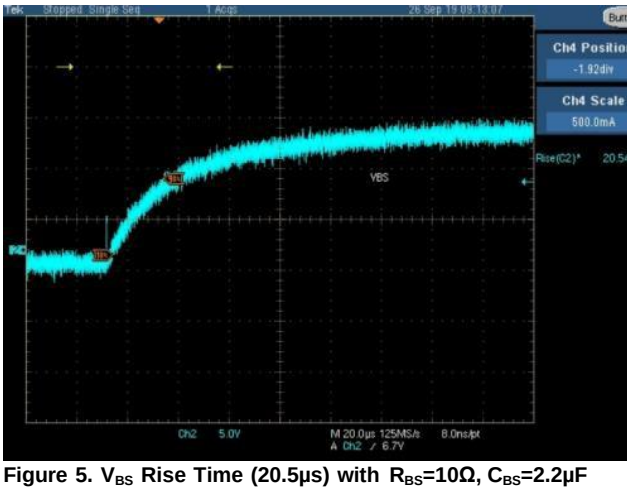

Figure 5. V_{BS} Rise Time (20.5µs) with R_{BS}=10Ω, C_{BS}=2.2µF

Bootstrap Diode

The chosen bootstrap diode (D_{BS}) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the V_S node. The diode's current rating is simply the product of the total charge (QT) required by the HVIC (High-Voltage Integrated Circuit) and the switching frequency. An ultra-fast recovery diode is recommended to minimize any delay of charging the C_{BS} cap. A 1A ultra-fast recovery diode is typical for DGD2003 applications.

Bootstrap Capacitor

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage (V_{GS_min}) must be greater than the UVLO of the high-side circuit, specifically for the V_{BSUV-} level. Therefore, if V_{GS_min} is the minimum gate-source voltage such that:

$V_{GS\_min} > V_{BSUV-}$

Then:

$\Delta V_{BS} = Vcc - V_f - V_{GS\_min} - V_X$

Where:

- Vcc is the supply voltage to the DGD2003
- V_f is the voltage drop across the bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET

V_X is calculated as the current seen across the low-side MOSFET multiplied by its R_{DS_ON}, and is simply V_{CE_ON} at the specific output current if an IGBT was used instead.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, the charge required to turn on the power devices, and duration of the high-side on-time. The total charge (QT) required by the Gate Driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{H\_ON}$

Where:

Q_G = gate charge of power device

Q_{LS} = level shift charge required per cycle

T_{H_ON} = high-side on-time

I_{LK_N} = sum of all leakages that include:

- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{Q_BS}: Quiescent current for high-side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet. Depending on the process technology, it can range anywhere from 3-20nC for 500V, to 1200V process respectively. Assuming a value of 10nC for the 200V process, it should be sufficient with added margins.

From the basic equation, the minimum bootstrap capacitor is then calculated as:

$$C_{B\_min} \geq Q_T / \Delta V_{BS}$$

Example Using a MOSFET

- Power Device = DMNH6021SK3Q
- HVIC = DGD2003
- Vcc = 12V
- Q_G = 20nC
- I_{GSS} = 100nA
- T_{H_ON} = 10µs
- $R_{DS(ON)}$ = 25mΩ max, 125˚C
- Iout = 5A
- I_{Q_BS} = 100µA
- I_{LK_IC} = 50µA
- Q_{LS} = 10nC
- V_F = 1.0V
- I_{LK_DB} = 100µA
- V_{GSmin} = 10.0V

From equations:

ΔV_{BS} = 12V- 1.0V-10V-(0.125V) = 0.875V

$Q_T = Q_G + Q_{LS} + (I_{LK\_N} * T_{H\_ON})$ where $I_{LK\_N} * T_{H\_ON}$ = 2.5nC

= 20nC + 10nC + 2.5nC

= 32.5nC

Thus, C_{BS} min = 32.5nC/0.875V = 37nF.

The bootstrap capacitor calculated in the above example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used. Utilizing values lower than this may result in overcharging of the bootstrap capacitor, especially during $-V_S$ transients.

Typically for motor driver applications, C_{BS} = 1µF to 10µF are used. It is also recommended to use low-ESR ceramic capacitors and to place them as close as possible to the V_B and V_S pins (see PCB Layout Suggestions).

Gate Resistor Component Selection

The most crucial time in the gate drive is the turning on and turning off of the MOSFET. Performing this function quickly with minimal noise and ringing is key. Too fast a rise/fall time may cause unnecessary ringing and poor EMI. Too slow a rise/fall time may cause an increase in switching losses for the MOSFET.

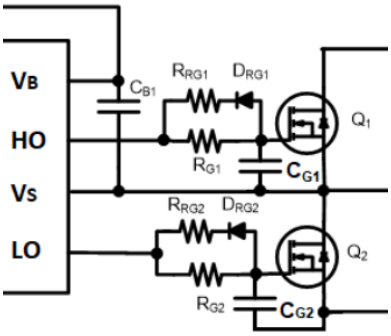

Figure 6. Gate Drive High-Side and Low-Side Components for DGD2003

Considering the Gate Driver components for DGD2003 in Figure 6, with the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise and fall times of the gate driver. For turning on, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn-off current flows from the MOSFET gate capacitor, through R_{RG1} and D_{RG1}, to the driver in the IC, to V_S for High-Side and COM for Low-Side. So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} are used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances. Hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing and poorer EMI, yet better efficiency, versus a slower rise time with better EMI and better noise performance, but poorer efficiency. The exact value depends on the parameters of the application. Generally for motors where the switching speed is slower and the application has more inherent noise, higher values are recommended; for example RG = 20Ω - 100Ω.

To have equal switching times for High-Side and Low-Side, it is recommended that the Gate Driver components for the high-side and low-side are mirrored. For example, $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{RG2}$, and $R_{G1} = R_{G2}$.

The gate-to-source capacitors, C_{G1} and C_{G2}, are used to minimize unexpected shoot-through in the Half-Bridge. This shoot-through can decrease efficiency or even damage the MOSFETs (discussed further in Unexpected Shoot-Through with dV_{DS}/d_t).

V_{CC} Decoupling Capacitor Selection

For optimal operation, Vcc decoupling is crucial for all Gate Driver ICs. With poor decoupling, larger Vcc transients will occur at the IC when switching. For greater and longer Vcc drops, the IC can go into UVLO.

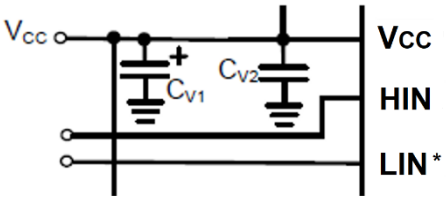

Figure 7. Suggested V_{CC} Decoupling

As shown in Figure 7, two decoupling capacitors are recommended: C_{V1} and C_{V2}. C_{V1} can be a larger electrolytic (for example 47µF), 50V, and is used to dampen low frequency drains on the supply. C_{V1} does not need to be placed right next to the IC. C_{V2} is used to decouple faster edge changes to Vcc and should be a low-ESR ceramic capacitor that is placed close to the Vcc pin. This component provides stability when Vcc is quickly pulled down with the load from the IC; typical values are 0.1µF to 1µF.

For applications with multiple Gate Driver ICs (for example BLDC motor drive with 3x Gate Drivers, as shown in Figure 1), one larger electrolytic (C_{V1}) can be used and the three ceramic caps (C_{V2}, C_{V3}, C_{V4}) should be placed close to the Vcc pin (see PCB Layout Suggestions)

High-Voltage Decoupling Capacitors

Considering the performance of the whole Half-Bridge, it is important to have the appropriate high-voltage decoupling capacitors (see C_{HV1}, C_{HV2}, C_{HV3}, and C_{HV4} in Figure 1). For the best stability (best high-frequency performance), C_{HV2}, C_{HV3}, and C_{HV4} are small ceramic capacitors (say, 1µF and 450V) that are placed close to the drain of the MOSFETs at the Half-Bridge (less than 25mm); and C_{HV1} is the electrolytic bulk capacitor that is typically part of the on-board power supply. For optimal operation if the small decoupling capacitors (C_{HV2}, C_{HV3}, and C_{HV4}) are not used, the bulk capacitor (C_{HV1}) should be placed close to the drain of the MOSFETs (less than 25mm).

Startup Sequence

To ensure that the Absolute Maximum Specifications for the inputs are met (see Figure 8), a correct startup sequence should be followed. The inputs cannot go above V_{CC}, hence V_{CC} should be powered up first before any signal is applied to HIN and LIN*. To enable the outputs to follow the inputs at startup, V_{CC} should be greater than UVLO+ (8.9V typ.) before any PWM signal is applied to the inputs.

Logic Input Voltage (HIN and LIN*)	V_{IN}	-0.3 to V_{CC}+0.3	V

Figure 8. Absolute Maximum Specification for Input Pins

Input Resistors

The IC PWM inputs, HIN and LIN*, are very high impedance inputs with a pull-down resistor (HIN) to COM, and a pull-up resistor (LIN*) to an internal 5V supply (see Figure 9). The pull-down resistor on HIN has a value of 1.5MΩ and the pull-up resistor on LIN* has a value of 1.5MΩ.

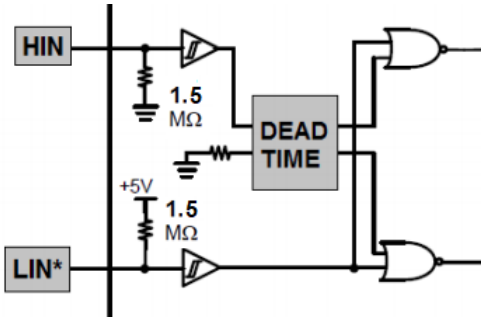

Figure 9. Input Logic for DGD2003

The DGD2003 will function with the HIN and LIN* pins tied together using only a single input. In this configuration, the input logic will insert a deadtime of 420ns to ensure that there is a deadtime between LO falling and HO rising, as well as HO falling and LO rising (to prevent shoot-through for MOSFETs).

Please note that because of the pull-up and pull down, and when HIN and LIN* are tied together but left open, the voltage on the input will be about 2.5V. In this situation, HO will turn on and LO will turn off, but it is near the threshold and not recommended to operate there. Hence if HIN and LIN* are tied together, it is recommended for the MCU output to be either high (for example 3.3V) or pulled low and not left open.

Matching Gate Driver with MOSFET or IGBT

IC Drive Current and MOSFET/IGBT Gate Charge

Gate Driver ICs are defined by their output drive current, which is their ability to source current to the gate of the MOSFET/IGBT at turn-on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2003, the drive current is I_{O+}=290mA typical and I_{O-}=600mA typical.

For a given MOSFET/IGBT with the known drive current of the DGD2003, the user may can calculate how long it will take to turn on/off the MOSFET/IGBT with the following equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the Gate Driver IC
t = calculated rise/fall time with the given charge and drive current

For example, with Diodes Incorporated's (Diodes) DMT10H010LK3, 650V IGBT: Qg = 33nC.
With the DGD2003 I_{O+}/I_{O-}, tr = 113ns and tf = 55ns.

These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, the addition of a gate resistor will increase the tr and tf.

Unexpected Shoot-Through with dV_{DS}/d_t

Unwanted MOSFET turn-on, from C_{GD} x dV_{DS}/d_t (see Figure 10), is often the cause of unexplained shoot-through in the Half-Bridge circuit. Depending on the ratio of the C_{GS}/C_{GD}, when the dV_{DS}/d_t across the low-side MOSFET (Q2) occurs (i.e. when the high-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, which turns on Q2 and causes shoot-through. In effect, a gate bounce occurs, causing ringing on the V_S line and the power ground.

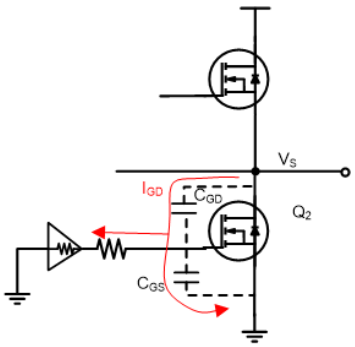

Figure 10. Unexpected Shoot-Through with dV_{DS}/d_t

Considering Figure 10,

$I_{GD} = C_{GD}$ x dV_{DS}/d_t

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the Gate Driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the C_{iss}/C_{res} in the MOSFET datasheet (C_{iss}/C_{res} gives an indication of C_{GS}/C_{GD}); having a C_{iss}/C_{res} as large as possible will minimize this phenomenon. An external capacitor can be added to the gate-source of the MOSFET (for example 1nF), which will increase C_{GS}/C_{GD}.

Minimum Pulse Requirement

The DGD2003 has an RC filter on the input lines to be more resilient in noisy environments. With a rising edge at the input to the Gate Driver, and then after the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the Half-Bridge will turn on and produce a bus voltage at the output. This MOSFET turn-on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure that turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2x deadtime for Half-Dridge Gate Drivers; hence for the DGD2003, the minimum pulse recommended at the logic inputs is 840ns.

During typical operation, the DGD2003 will respond to an input pulse greater than about 420ns (typical value of deadtime); this is due to the deadtime logic and input logic of the DGD2003. Hence for an input pulse greater than approximately 420ns, the IC will follow the pulse as expected. For an input pulse of less than 420ns, there will be no response from the IC.

PCB Layout Suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation, which can arise from a poor layout of the associated components. Figure 11 shows a schematic with parasitic inductances in the high-current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}), which would be caused by inductance in the metal of the trace. Considering Figure 11, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible, as well as using low-ESR ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce parasitics due to the PCB traces.

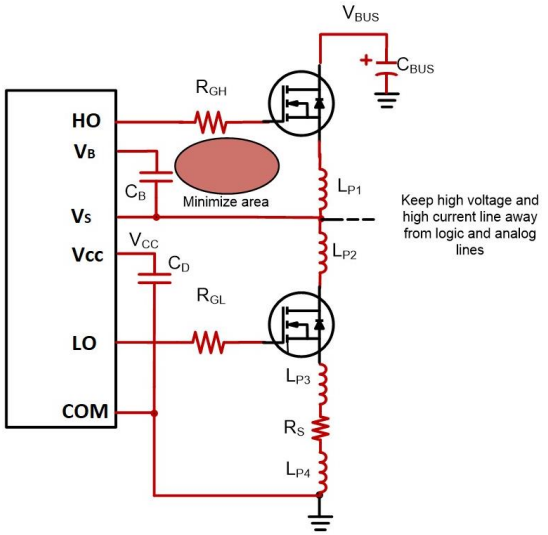

Figure 11. Layout Suggestions for DGD2003 in a Half-Bridge (lines in red should be as short as possible)

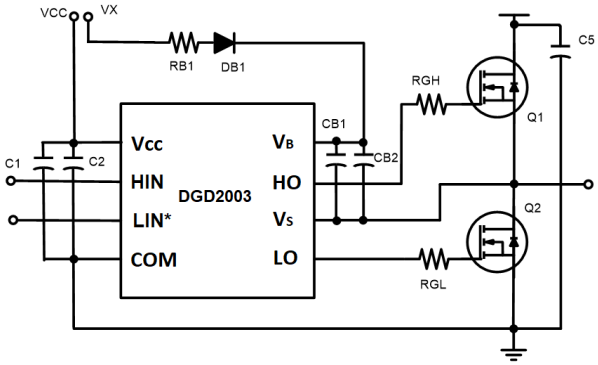

Figure 12. Schematic for Layout Example in Figure 13

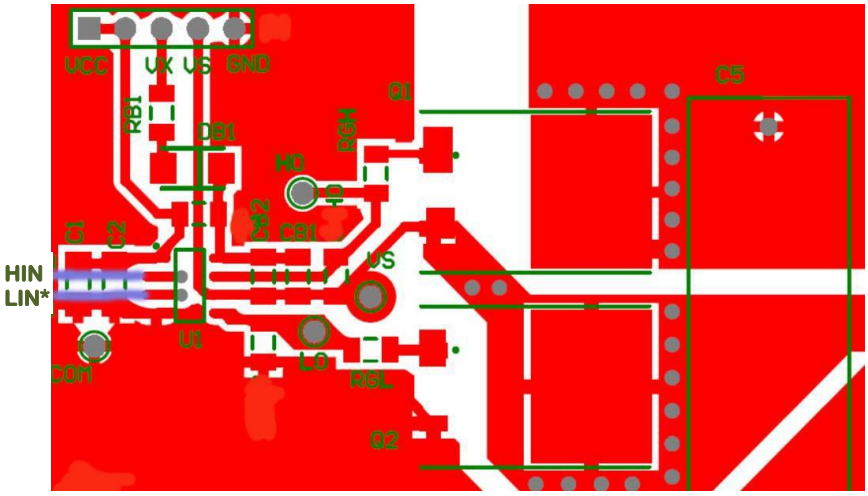

Figure 13. Layout of the Schematic Shown in Figure 12, DGD2003 in SO-8 (all routing and components on top side except for HIN and LIN* from input.

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