Replacing the Intel 21150 or PLX PCI6150 with the PI7C8150

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1.0 Introduction

The PCI bus has been used for more than fifteen years and is still running strong. This interface is being developed in PCs, Servers, Notebooks, Datacom and Telecom Systems. With many different PCI devices and peripherals being placed in systems today, the need for PCI Bridges becomes essential.

Pericom Semiconductor Corp. has a broad selection of PCI to PCI bridges, including the PI7C8150 , PI7C8150 A, and the PI7C8150 B. This application note discusses the differences between the Pericom bridges and the PLX 6150 and the Intel 21150

2.0 Pin differences

1. The following are the pin differences for the PQFP package

Pin Number	Pericom PI7C8150/ A	PLX 6150/ HB4	Comments
51	VDD	Osc_Sel_L	Connect to VDD to work in Synchronous mode. To work in Async mode Plz see the PI7C8150B
54	VSS	Osc_In	Tie to Ground To work in Synchronous mode.
103	VDD	EE_En_L	Tie High to disable the Serial EEPROM function. The PI7C8150A does not support this EEPROM feature
106	MS1	Eject_En_L	Tie to Ground to work in Synchronous mode. The PI7c8150 A does not support Hot swap
127	Reserved	Enum_L	Hot swap signal, NO connect is OK. The PI7C8150 A does not support Hot swap
128	Reserved	LED	Hot swap signal, NO connect is OK. The PI7C8150 A does not support Hot swap
151	VDD	Reserved	Connect to VDD for normal operation
155	MS0	GPIO3_FN_L	Connect to VDD for normal operation
158	VSS	EEPCLK	Connect to Ground. The PI7C8150A does not support this EEPROM feature
160	VSS	EEPD	Connect to Ground. The PI7C8150A does not support this EEPROM feature

Pin Number	Pericom PI7C8150/ A	Intel 21150	Comments
106	MS1	VSS	No change required
127	Reserved	NC	No change required
128	Reserved	NC	No change required
155	MS0	VDD	No change required

2. The following are the pin differences for the BGA package

Ball Number	Pericom 8150 /A	PLX 6150/HB4	Comments
K16	CFG66 SCAN_EN_H	OSC_SEL_L	Connect to VDD to work in Synchronous mode. To work in Async mode Plz see the PI7C8150B
K15	MSK_IN	OSC_IN	Tie to Ground To work in Synchronous mode. To work in Async mode Plz see the PI7C8150B
C15	VDD	EE_EN_L	Tie High to disable the Serial EEPROM function. The PI7C8150A does not support this EEPROM feature
R16	MS1	EJECT_EN_L	Tie to Ground To work in Synchronous mode. The PI7C8150 A does not support Hot swap
J14	Reserved	ENUM_L	Hot swap signal, NO connect is OK. The PI7C8150 A does not support Hot swap
J16	Reserved	LED	Hot swap signal, NO connect is OK. The PI7C8150 A does not support Hot swap
B14	MS0	GPIO3FN_	Tie High to work in

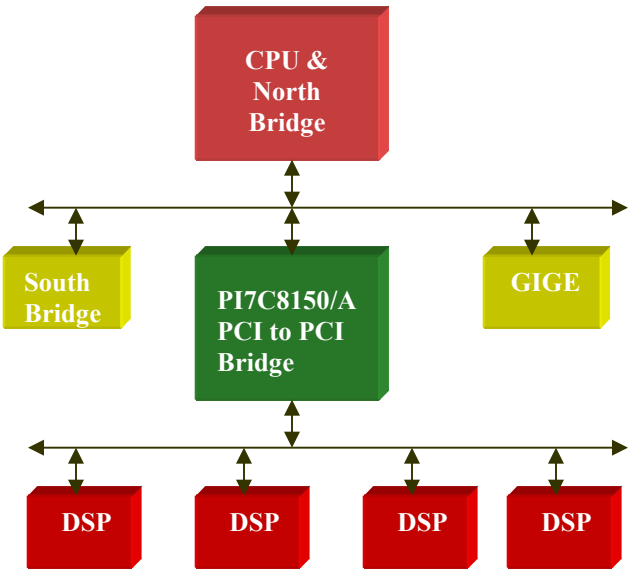
		L	Synchronous mode
C14	VSS	EEPCLK	Connect to Ground. The PI7C8150A does not support this EEPROM feature
D14	VSS	EEPD	Connect to Ground. The PI7C8150A does not support this EEPROM feature

Ball Number	Pericom PI7C8150/ A	Intel 21150	Comments
R16	MS1	VSS	No change required
J14	Reserved	NC	No change required
J16	Reserved	NC	No change required
B14	MS0	VDD	No change required

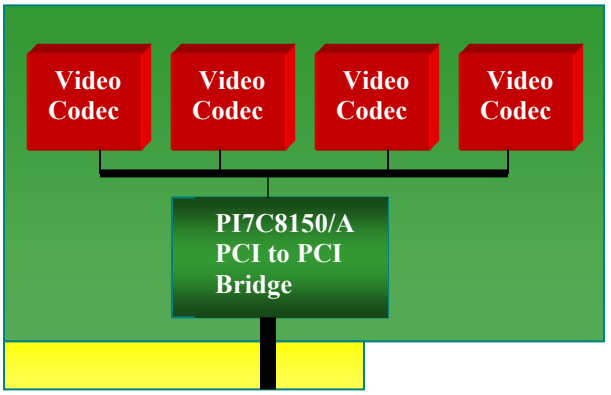
3.0 Applications

The PCI to PCI Bridge is used in the following applications:

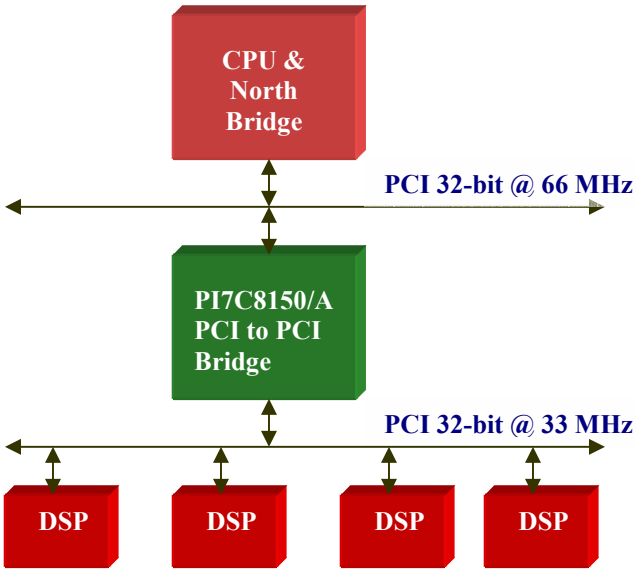
3.1 Bus Expansion. On the motherboard, in order to add more slots.



3.2 On the Add_ in cards if there is more than one PCI load.



3.3 Bus isolation in order to isolate the high-speed devices from the lower speed chips.



4.0 Unique features

Apart from pin differences, the 8150/A has many enhanced features:

4.1 Industrial Range

The chip is also offered in industrial range. This feature will enable the designer to place the chip in extreme temperature range as low as – 40 Celsius and as hot as + 85 degrees Celsius. If the chip is not used in this extreme environment, this feature will provide plenty of AC timing margin.

4.2 Optimum FIFO size

Pericom has experimented with many different numbers of write and read FIFO's. The Analysis was done on many different applications. Our Analysis indicated that we need the following FIFO size to achieve the best performance:

- 512 bytes delayed read transaction FIFO's for both the primary and the secondary sides.
- 256 bytes of posted write buffers for both the primary and the secondary sides.

The data indicated that bigger FIFO's are not necessarily better. You have to choose the right number in order to service both the write and the read transactions. This Architecture proved to be the optimum based on the performance report, which is also provided on the web site for your convenience.

4.3 Dynamic Prefetching

This is a unique feature that is integrated into the bridge. As you know in the PCI bus writes go fast, since most every device have a buffer where they immediately accepts the writes without adding many wait states. Read Transactions are more complex. Normally reads take much longer time. The bridge has to flush the write buffers and then request the read form the destination chip. The chip also can get one cache line or many cache lines. Usually the user does not know how many it needs since it depends on the chipset that is used and the application. The 8150A have a feature that automatically adjusts to the optimum number of cache line reads in order to match the requested reads. This will result in better performance and better utilization of the bus so that we do no waste the bus bandwidth and read extra transactions to discard them later. On the other hand we will not read less read transactions then needed so that we will starve the initiator that is requesting the read transactions.

5.0 Conclusion

The 8150 /A have many superior features to the competition and it is also Pin to pin compatible so that it will fit into a socket that is designed for the competition.
The 6150/HB4, the 21150 and the 8150 / A chips are pin-to-pin compatible. There are minor pinout differences between them. If you are not using the Serial EEROM feature and the hot swap pins then the Pericom PI7C8150/A can be dropped in into the 6150 or the 21150 Socket. If you are doing an asynchronous design then you will need to use the PI7C8150 B.