Hardware Implementation Guide for the PI7C8152

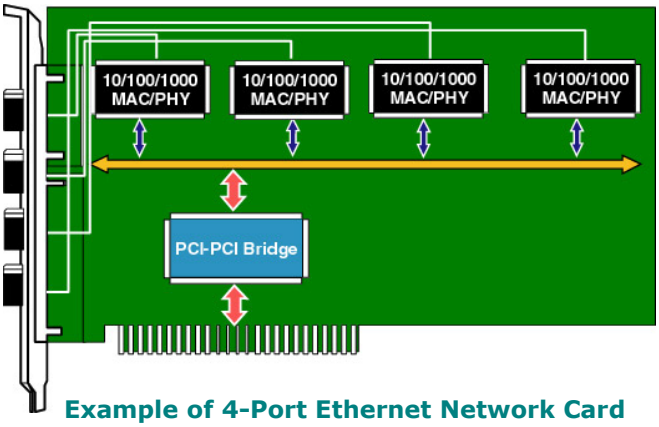
By Glenn Sanders

Introduction

The PCI interface was originally created for the personal computing industry. These days it has been adapted by system designers who incorporate it into Datacom, Telecom, PCs, Servers, and many other systems. Currently the PCI interface is used mainly as an expansion bus to add PCI slots on the system motherboards that have wide ranging applications. It is also used in add-in cards since most systems have PCI slots available to insert the PCI add-in cards. The PI7C8152 PCI-to-PCI Bridge is a 32-bit, 66 MHz capable chip that can be used either within an add-in card or on a motherboard.

Schematic and Layout Guidelines

This section has guidelines for hardware implementation of the Pericom PI7C8152 PCI-to-PCI Bridge (8152) in an add-in card or system motherboard.



Example of 4-Port Ethernet Network Card

Power

The 8152 bridge supports both 3.3V and 5V signaling environments. The chip core is powered by 3.3V Vdd and signaling on either bus is at the voltage level of the respective P_VIO (pin 67) or S_VIO (pin 52) inputs.

Clock Frequency

Regardless of the status of M66EN (PCI connector signal 49B) at either PCI bus, the input clock frequency at signal P_CLK will always be the frequency used for S_CLOCKOUT[0:4]. A motherboard with PCI slots might have any speed device inserted, but an add-in card usually has embedded devices. Therefore an add-in card with appropriate 66 Mhz PCI capable devices could be designed to 66 Mhz tolerances, and function in both 33 and 66 Mhz environments using the low cost PI7C8152 rather than higher pin count/cost alternative model bridges.

Miscellaneous signal connections

For 8152 IC:		
Pin name	**location**	**Requested value**
S_SERR_L	Pin 3	Pull high to Vdd through 5.1K ohm resistor
S_PERR_L	Pin 4	Pull up
S_LOCK_L	Pin 5	Pull up
S_STOP_L	Pin 6	Pull up
S_DEVSEL_L	Pin 7	Pull up
S_TRDY_L	Pin 9	Pull up
S_IRDY_L	Pin 10	Pull up
S_FRAME_L	Pin 11	Pull up
SCAN_TM_L	Pin **63**	Pull up
SCAN_EN	Pin **62**	Can be NC (no connect)
S_CFN_L	Pin 49	Tie low for secondary bus internal arbiter; pull high for external arbiter. For more details see page 4.
BPCCE	Pin 159	Tie low if not using power management; pull up to enable power management
For **each PCI** slot:		
Pin name	**location**	**Requested value**
REQ#		Pull high to Vdd through external resistor
ACK64#		Pull up
REQ64#		Pull up
SDONE	(A40)	Pull up
SBO#	(A41)	Pull up

Output Clocks

Each secondary clock output is limited to one load. One secondary clock output is used to feedback into S_CLKIN, with the remaining 4 clocks driving embedded PCI devices/slots.

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

All secondary clock traces including feedback should have the same length so as to deliver the clock at the same time at their respective destinations. This means that the furthest secondary bus device from the bridge governs the effective secondary bus clock trace lengths. Unused clock outputs can be disabled by writing to the bridge configuration register at offset 68h, or terminated electrically.

Clock lines are best terminated with a series termination resistor. The value to use depends on the impedence of your transmission lines. Our 65 ohm trace impedence reference board uses 22 ohm resistors placed close to the bridge; some designs use as little as 10 ohms and others as much as 33 ohms, with 50 ohm to 75 ohm trace impedences. could be bused from each PCI connector then routed around our bridge out to the primary PCI bus with some pull up resistor.

3.3Vaux This power source, if implemented on your design, should be bused from the primary PCI connector around the bridge to the secondary bus connectors.

Power Decoupling

In order to reduce noise at Vdd or ground from impacting the bridge, place 4 sets of decoupling capacitors top and bottom as close as possible to each corner of the bridge IC. These should be {0.1 uF, 0.01 uF, 0.001 uF} on bottom side and be {10 uF, 0.1 uF, 0.01 uF, 0.001 uF} top side. These are in addition to further decoupling at the PCI primary interface and secondary slots as needed per PCI spec 2.2 sec. 4.4.2.1 "***power decoupling***".

For add-in cards, please add the following decoupling capacitors at the edge connector, for 3.3V and 5V pins, with values {0.1 uF, 0.01 uF, 0.001 uF}. Use high quality, low ESR surface mounted ceramic capacitors.

PCI INTERRUPTS

PCI interrupts are processed at the motherboard south bridge, which sits on the primary PCI bus (thus upstream from the 8152). Thus there aren't signals at the bridge for interrupt processing; rather during layout the board designer routes the INTA#, INTB#, INTC#, and INTD# signals directly to the corresponding signals on the primary bus.

When the secondary bus is to have PCI connectors, the pin position of the PCI INTx# signals rotates from slot to slot., per PCI 2.2 spec 2.2.6 (page 14).

Six layer board stacking recommendation

For **5V** or mixed signaling environments, we recommend a 6 layer board arranged as follows:

Top	route clock and other critical signals on top
Internal plane 1	Ground
Internal plane 2	3.3 V
Internal plane 3	5 V (with 12V islands)

There is no clock programming circuit required by hardware; normally all secondary clock outputs are enabled. Likewise there are no GPIO pins, JTAG scan port.

BPCCE: bus power/clock control enable (pin 159)
This signal can be in either state (high or low) and your design will work under normal conditions. The one thing you should NOT do is let this or any other INPUT signal float.

Additional PCI signals per PCI specification 2.2, section 2.2.7: PRSNT[1:2] Normally these are pulled high with a decoupling capacitor to ground on the secondary bus.

PME# Power Management Event signal, an optional signal. The 8152 doesn't have a dedicated PME# pin, so this Internal plane 4 Ground Bottom signal connections

Do NOT route high frequency bus signals under the bridge.

Signal layers should be seperated by ground planes, and no signals routed between ground and power planes. Use FR-4 material for board fabrication.

General layout guidelines:

1. Limit your trace lengths. Longer traces display more resistance and induction and introduce more delays. It also limits the bandwidth which varies inversely with the square of trace length.
2. Use higher impedence traces. Raising the impedence will also increase the bandwidth. Per PCI specification 2.2 section 4.4.3.3 trace impedence should be controlled to be within 60 to 100 ohms range.
3. Do not use any clock signal loops. Keep clock lines straight when possible.
4. For related clock signals that have skew specifications, match the clock trace lengths.
5. Do not route signals in the ground and Vcc planes.
6. Do not route signals close to the edge of the PCB board.
7. Make sure there is a solid ground plane beneath the bridge IC (PI7C8152).
8. The power plane should face the return ground plane. No signals should be routed between power and ground.
9. Route clock signals on the top layer and avoid vias for these signals. Vias change the impedence and introduce more skew and reflections.
10. Do not use any connectors on clock traces.
11. Use wide traces for power and ground.
12. Keep high speed noise sources away from the PI7C8152.
13. Remember that per PCI spec 2.2 sec 4.4.3.1, the PI7C8152 should have a primary PCI edge connector to PQFP pad trace distance of not more than 1.5 inches (37.5 mm) for signals coming from the primary PCI interface. Secondary interface signals would then be limited as in PCI motherboard layout rules.

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

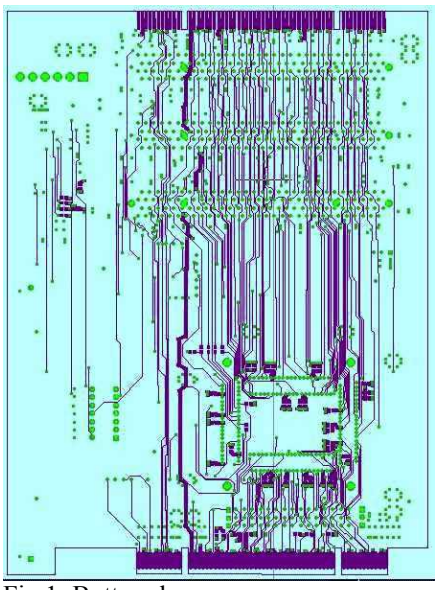


Fig 1: Bottom layer

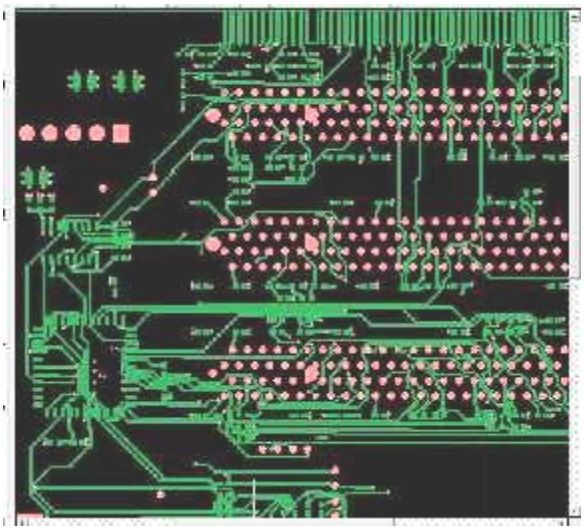


Fig 2: Detail of top layer near external arbiter clock and req/gnt enter at lower left

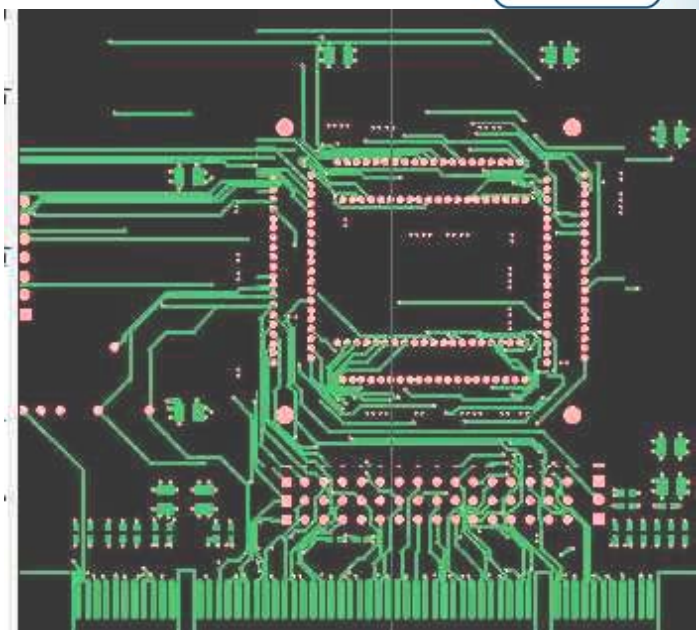


Fig 3: Detail of top layer with mechanical socket at bridge

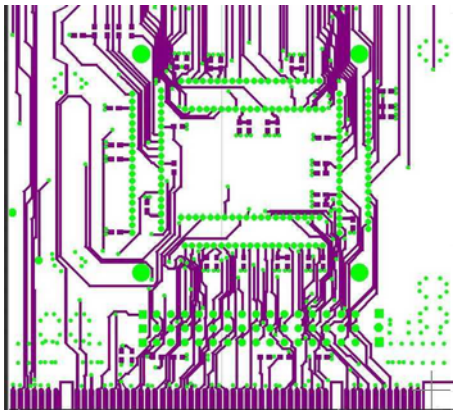


Fig 4: Detail of bottom layer

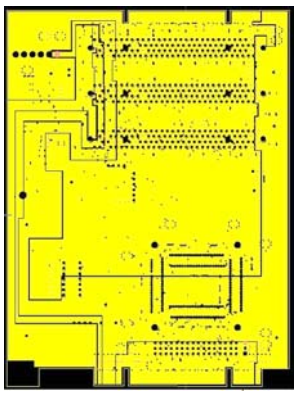


Fig. 5a: 5V layer (with 12V islands)

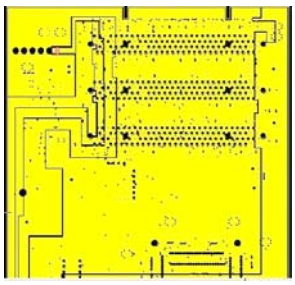


Fig 5b: detail *note –12V and +12V islands*

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com

External Arbiter

An arbiter needs to watch the PCI bus clock, each REQ#, and the control signals RESET#, TRDY#, DEVSEL#, LOCK#, STOP#, FRAME#, CBE[3:0] and IRDY#. The 8152 normally uses an internal abiter for the secondary PCI bus. However there exists a method to use an external arbiter:

In order to **disable** the internal arbiter, tie **high** (pin 49) S_CFN_L.

Next the bridge needs to output a REQ# and wait for a GNT# input just like any other bus master device. When the bridge is in the internal arbiter mode, it waits to receive as inputs REQ#s from bus master devices on the secondary bus and then issues as an output a corresponding GNT#. Now that the bridge is yet another device, it must output a REQ# to the external arbiter and wait its turn to use the bus, which will be an input GNT# signal. The signal named **S_GNT_L[0]** (pin 43) will become the bridge REQ# on the secondary bus, since it is an output from the bridge, in external arbiter mode. Signal name **S_REQ_L[0]** (pin 37), as it is an input, will be the bridge GNT# on the secondary bus when in external arbiter mode.

Finally, route the S_REQ_L[3:0] traces from the PCI slot connectors/embedded devices to the external arbiter. Route the S_GNT_L[3:0] devices likewise. At the 8152 bridge, the inputs S_REQ_L[3:0] **do not** have any internal pullups, so the signals S_REQ_L[3:0] need pull ups at the inputs to the bridge. As GNT#s are normally output by the bridge, the S_GNT#[3:0] can also be left as no connect in external arbiter mode.

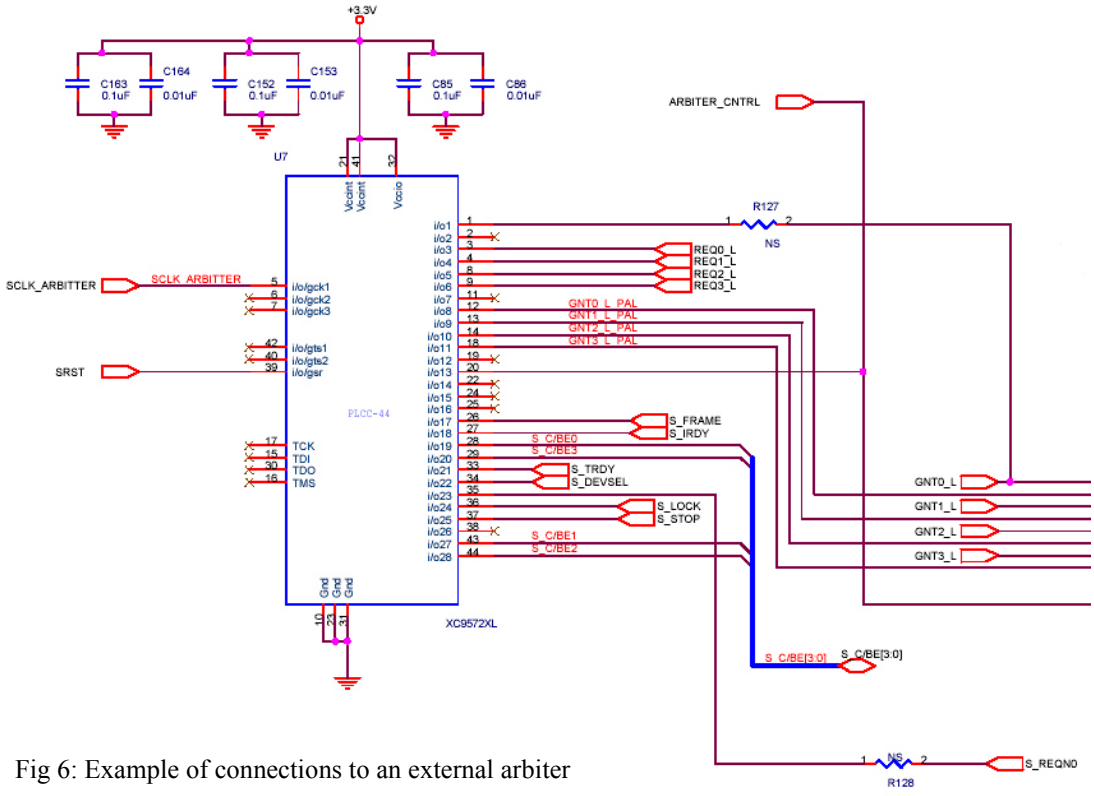


Fig 6: Example of connections to an external arbiter

References

1) Pericom Semiconductor App Note #22 "*Solutions to Current High-Speed Board Design*"

2) PCI Local Bus specification 2.2 section 4.4 "*Expansion Board Specification*" [*decoupling* through *routing recommendations* and *impedence* sections] p150-152.

3) PCI Local Bus specification 2.2 section 4.2.6 *Pinout recommendation* p131.

4) PCI Local Bus specification 2.2 section 4.3.3 *Pull-ups* p136.

5) Compact PCI PICMG 2.0 R3.0 p17-20 "*Electrical Requirements*"

6) Pericom semiconductor App Note #31 "*Zero-Delay Clock Buffer Layout and Schematic Guidelines"* p1.

Pericom Semiconductor ▪ 2380 Bering Drive ▪ San Jose, CA 95131
PH: 800-435-2336 FX: 408-435-1100
www.pericom.com